Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for providing a synchronized ~~system~~ clock signal having reduced jitter ~~in a system having a received PN clock signal, said synchronized system clock signal being synchronized with said received PN clock signal~~, the method comprising ~~the steps of~~:

receiving ~~providing~~ a stable high frequency reference signal;

dividing said high frequency reference signal which allows a ~~system~~ clock signal to have one of a plurality of ~~system~~ clock phases;

~~recovering said received~~ receiving a pseudorandom number (PN) clock signal ~~by~~ and providing PN phase adjustments of said received PN clock signal;

generating a tracking control signal in response to said PN phase adjustments for adjusting said ~~system~~ clock phase to one of the plurality of available phases; and

adjusting said ~~system~~ clock phase in accordance with the tracking control signal to provide said synchronized ~~system~~ clock signal.

2. (Previously Presented) The method of claim 1, wherein said tracking control signal indicates the amount of the adjustment to make to said ~~system~~ clock phase, wherein said adjustment can be in the positive or negative direction

3. (Previously Presented) The method of claim 1, wherein the tracking control signal indicates the number of adjustments to make to said ~~system~~ clock

phase, wherein said adjustment can be in the positive or negative direction.

4. (Cancelled)

5. (Currently Amended) The method of claim 1 further comprising: ~~the step of~~

multiplying said high frequency reference signal prior to dividing said high frequency reference signal.

6. (Original) The method of claim 1 wherein said high frequency signal is provided using a temperature compensated crystal oscillator.

7. (Currently Amended) A base station (BS), ~~communication system for providing a synchronized system clock signal having reduced jitter, said system having a received pseudorandom number (PN) clock signal, said synchronized system clock signal being synchronized with said PN clock signal~~, the BS ~~system~~ comprising:

circuitry configured to ~~provide~~ receive a stable high frequency reference signal;

a divider to divide said high frequency reference signal which allows a ~~system~~ clock signal to have one of a plurality of ~~system~~ clock phases;

circuitry configured to ~~recover said received~~ receive a pseudorandom number (PN) clock signal and to provide ~~by providing~~ PN phase adjustments of said received PN clock signal;

circuitry configured to generate a phase adjustment signal to adjust ~~for adjusting~~ a ~~system~~ clock phase to one of the plurality of available phases; and

circuitry configured to adjust said ~~system~~ clock phase in accordance

with the phase adjustment signal to provide said synchronized ~~system~~ clock signal.

8. (Currently Amended) The ~~system~~ BS of claim 1 wherein said tracking control signal indicates the amount of the adjustment to make to said ~~system~~ clock phase, wherein said adjustment can be in the positive or negative direction

9. (Currently Amended) The ~~system~~ BS of claim 1, wherein the tracking control signal indicates the number of adjustments to make to said ~~system~~ clock phase, wherein said adjustment can be in the positive or negative direction.

10. (New) A remote network terminals (RNT), the RNT comprising:

circuitry configured to receive a stable high frequency reference signal;

a divider to divide said high frequency reference signal which allows a clock signal to have one of a plurality of clock phases;

circuitry configured to receive a pseudorandom number (PN) clock signal and to provide PN phase adjustments of said received PN clock signal;

circuitry configured to generate a phase adjustment signal to adjust a clock phase to one of the plurality of available phases; and

circuitry configured to adjust said clock phase in accordance with the phase adjustment signal to provide said synchronized clock signal.

11. (New) The RNT of claim 1 wherein said tracking control signal indicates the amount of the adjustment to make to said clock phase, wherein said adjustment can be in the positive or negative direction

12. (New) The RNT of claim 1, wherein the tracking control signal

indicates the number of adjustments to make to said clock phase, wherein said adjustment can be in the positive or negative direction.